(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 144 779**
A2

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 84113431.5

(22) Date of filing: 07.11.84

(51) Int.Cl.⁴: G 06 F 9/44

(30) Priority: 07.11.83 JP 208567/83

(43) Date of publication of application:
19.06.85 Bulletin 85/25

(84) Designated Contracting States:
AT BE CH DE FR GB IT LI LU NL SE

(71) Applicant: Sowa, Masahiro
232-3, Hakoda-Cho
Maebashi-shi Gunma-ken(JP)

(71) Applicant: OMRON TATEISI ELECTRONICS CO.
10, Tsuchido-cho Hanazono Ukyo-ku
Kyoto 616(JP)

(72) Inventor: Sowa, Masahiro
232-3, Hakoda-cho
Maebashi-shi Gunma-ken(JP)

(74) Representative: WILHELMS & KILIAN Patentanwälte
Eduard-Schmid-Strasse 2
D-8000 München 90(DE)

(54) Parallel processing computer.

(57) A parallel processing computer comprises at least a memory for storing program as well as data and instructions for executing the program, a plurality of functional units, a node driving register for indicating executable instructions which are allowed to be executed by the functional units, and a mode register giving information to the functional unit as to whether the processing to be executed is of serial nature or parallel nature.

0 144 779 A2

0144779

BACKGROUND OF THE INVENTION:

FIELD OF THE INVENTION:

The present invention in general relates to a parallel processing computer system which performs processings in parallel at machine language level. In more particular, the invention relates to a parallel processing computer system which is additionally capable of executing operations on the basis of the principle adopted in the so-called Neuman type computer system, a typical one of serial or sequential processing computers.

DESCRIPTION OF THE PRIOR ART:

Most of the computers which are used at present are operative on the basis of the serial processing principle in accordance with the concept adopted in the Neuman type computer system. However, in view of the currently prevailing state in which the computers are employed increasingly in many and various industrial and commercial fields, there exists certainly a great demand for the availability of a computer which can perform processing at very high speed.

In this connection, it is noted that the Neuman type computer whose operation is based on the serial processing priciple is not inherently suited for the execution of processings which are required to be performed at ultra-high speed. For attaining the high speed processing as demand, the computer should be imparted with the capability for performing a plurality

of processings in parallel. Under the circumstances, studies and activities are now under way in an attempt to develope an ultra-high speed computer system which is based on the parellel processing principle. In reality, data flow computers, control flow parallel computers and others have already been proposed.

However, most of the hitherto known parallel processeeing computers suffer drawbacks that the sequence in which instructions are to be excuted can not be definitely determined in contrast to the Neuman type computer which is inherently designed to excute processings in a deterministic manner, the parallel processing computer may encounter difficulty in the processing of certain input signals so that corresponding output signals can be produced within a predetermined time. Moreover, the processsings which are intrinsically to be performed in series or sequence can not be executed by the parallel processing computer without lowering the operation speed in contradiction to the fact that the parallel processing computer has been developed with the aim to increase the operation speed.

Further, the parallel processing computer differs from the conventional computers of Neuman type in respect to the basic principle. So, there may arise such a situation that the replacement of the Neuman type computer by the parallel processing computer cannot be smoothly realized, particularly in the fields where a great amount of available softwares developed until now exert important influences to the efficiency of works to be accomplished by using computer. In other words, the parallel processing computer is incompatible with the Neuman type computer in respect to the available softwares.

SUMMARY OF THE INVENTION:

It is therefore an object of the present invention to provide a parellel processing computer which is so arranged as to be capable of performing serial processings in addition to parallel processings, not only non-deterministical processings but also deterministical processings, and further programs prepared for parallel processings, inclusive of serial processings, at such a high speed as that of Neuman type serial processing computer so arranged as to perform serial processings.

another object of the present invention is to provide a parallel processing computer which can make use of a great amount of currently available softwares so that the transfer orreplacement of the Neuman type serial processing computer by the parallel processing computer can take place smoothly.

In view of the above and other objects which will be more apprent as description proceeds, there is provided according to a general aspect of the invention a parallel processing computer which comprises at least a memory for storing data and instructions, a plurality of functional units, a node driving register means for indicating instructions which are allowedto be executed, and a mode register for indicating to each functional unit whether processing in concern is ofserial nature or parallel nature.

With the arrangement of the parallel processing computer described above, it is assumed that a given one of the functional units fetches an executable instruction from the memory which instruction is designated by one word contained in the node

driving register in the course of parallel processing which is represented by a mode identifier "P" placed in the mode register. In that case, when the instruction as read out indicates initiation of the serial processing (e.g. Neuman type processing), an identifier "N" representative of the serial or Neuman processing is loaded in the mode register. Thereafter, the one word of the node driving register is used only for the given functional unit mentioned above and serves as a program counter cooperate to perform the function corresponding to that of the central processing unit (CPU) of the Neuman type computer. When a return instruction is issued to the given functional unit, the latter as well as a part of the node driving register operating as the Neuman type computer is restored as the parts constituting the parallel processing computer, whereupon "P" is loaded in the mode register.

With the arrangement described above, the switching to the Neuman type or serial processing computer can be realized in a much simplified manner. Further, since a plurality of Neuman type computers can be simultaneously realized in single parallel processing computer, Neuman type program or programs can be executed simultaneously with the execution of a program for the parallel processing.

BRIEF DESCRIPTION OF THE DRAWINGS:

Fig. 1 shows in a block diagram a general arrangement of a parallel processing computer according to an exemplary embodiment of the invention; and

Fig.2 is a program graph for illustraing operation of the parallel processing computer shown in Fig.1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS:

In the first place, the principle on the basis of which the parallel processing computer according to the invention operates will be elucidated by referring to a program graph shown in Fig. 2.

Reference symbols N_1 to N_4 represent what is referred to as nodes which may be stored in a memory, and which contains contents to be processed. Arrows shown on the input side of each node are referred to as the onput arcs in accordance with graph theory while the outgoing arrows on the output side of each node are referred to as the output arcs.

The principle of this computer is that processing of the content placed in each node N is allowed to be executed only when tokens indicative of "control of execution" meaning whether said content of the node should be processed or not (shown in solid circle in Fig.2) are placed on all the input arcs of the node in concern. Upon completion of the processing by fetching the control tokens from the input arcs, another token is outputted on the output arc.

The token to be inputted to a given node constitutes a so-called token packet TP together with a node pointer NPR indicating the existence or address of the given node in the memory, the token packet being stored in a node driving register or NDR 1 described thereinafter. In Fig.2, LT represents a left token, and RT represents a right token.

In the case of the program illustrated in fig. 2, arithmetic operation is executed through the nodes N_1 to N_4 in accordance

with

$$y = \frac{a+b}{a \times b} + a + b$$

Now, referrence is made to Fig. 1 which shows a hardware architecture of a control flow parallel processing computer according to an embodiment of the invention. In the figure, a reference numeral 1 denotes the node driving register (NDR) mentioned above, 2 denotes mode registers (MD_1 to MD_n) for placing therein signals commanding the parallel processing or Neuman type processing, 3 denotes an assembly of functional units (FU_1, FU_2,...,FU_n) for performing the processings on the node basis, and 4 denotes a memory (M) for storing instructions to be executed at the nodes and data used for executing the instructions.

Assuming that all the mode registers MD_1, MD_2,.., MD_n contain the mode identifier "P" indicating the parallel processing mode, the functional units FU_1, FU_2,..., FU_n of the computer operate as follows.

At first, the functional units fetch from the node driving register 1 the token packets TP each containing enough tokens for executing the processing at the nodes (1st Step).

By way of example, assuming that the functional unit FU_2 fetches the token packet TP to be inputted to the node N_3 shown in Fig. 2 from the seventh word NDR (7) of the node driving register 1, the corresponding introduction and data designated by the node pointer NPR contained in the token packet are read out from the memory 4 (2nd Step).

Subsequently, arithmetic operation is carried out in accordance with, e.g. $x = p \div q$, under command of the instruction read out from the memory 4 by using the data also read out from said memory 4 (3rd step).

After the completion of the arithmetic operation, the output token to the node N_4 is combined with the node pointer designating the node N_4 (shown in broken line block in Fig.2) to thereby prepare a token packet TP which is then placed in the node driving register NDR 1as for example, 3rd word (3) (4th step).

The token packets written in the node driving register 1 and including the same node pointer NP are stored in a set (5th step).

Operations of the kind mentioned above are performed by the function units 3 independent of one another, whereby the program is executed in parallel.

Now, it is assumed that the instruction read out from the memory 4 at a certain step for executing the processing commands initiation of a Neuman type program (N BIGIN) as designated at the node N_5. Then, the functional unit FU_2 places the mode identifier "N" at the associated mode register MD_2, as the result of which the seventh word (7) of the node driving register 1 is allocated for use only by the functional unit FU_2. Thereafter, the node pointer region NPR of the seventh word (7) of the node driving register 1 serves as a program counter of the Neuman type computer. In other words, the seventh word (7) of the node driving register 1 constitutes a Neuman type computer together with the functional unit FU_2 and the mamory 4. The Neuman

type computer may then perform a Neuman type program illustrated in a dotted broken line block in Fig. 2. When the execution of the Neuman type program comes to an end, e.e. at the node N_6, as indicated by "N END", the functional unit FU_2 places the mode identifier "P" in the mode register MD_2, whereupon the node pointer area of the seventh word (7) of the node driving register 1 gets rid of the functional unit FU_2. Thus, the seventh word of the NDR 1 as well as the functional unit FU_2 are restored as the members constituting the parallel processing computer and may take parts in the execution of a succeeding parallel processing program.

In a version of the illustrated embodiment, a program counter may be previously incorporated in the functional unit so that the program couter can be used in response to the mode idintifier "N" placed in the associated mode register. Further, the illustrated parallel processing computer may serve as a data flow computer by employing data for the token.

Although the invention has been described in conjunction with the preferred embodiment, it should be appreciated that many modifications and variations will readily occur to those skilled in the art without departing from the spirit and scope of the invention.

CLAIMS

1. a parallel processing computer, comprising:

a node driving register imparted with at least a function for indicating executable instructions;

functional units for executing the instructions; and

a memory for storing programs;

wherein a word of said node driving register is temporarily allocated to the use only by a given one of said functional units and so controlled as to serve for a same function as that of a program counter of a Neuman type computer.

2. a parallel processing computer, comprising:

a node driving register imparted with at least a funtion for indicating executable instrucitons;

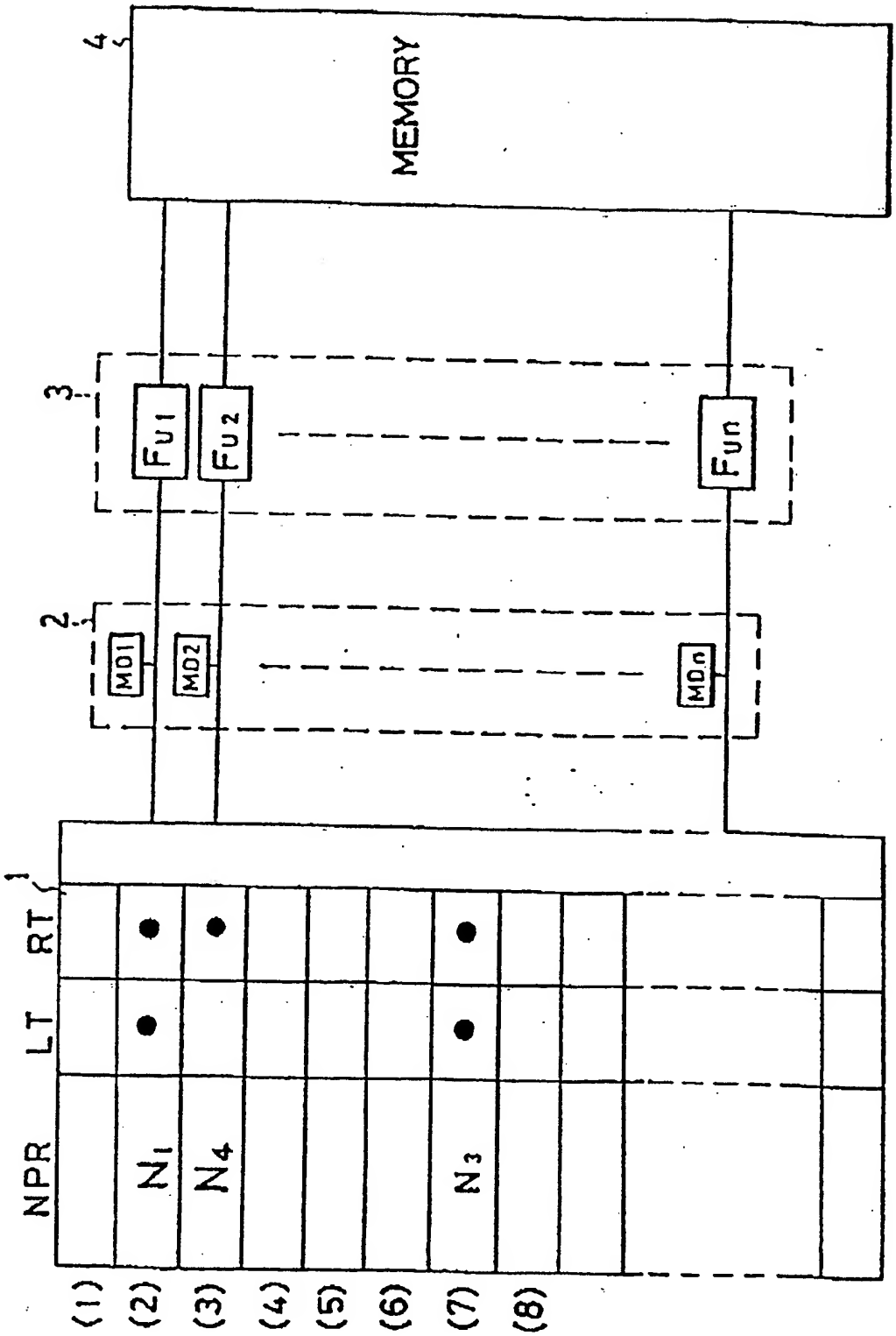
functional units for executing the instrucitons; and

a memory for storing programs;

wherein a program conter is incorporated in at least given one of said functional units so that a Neuman type program can be executed through cooperation of said program counter, said given functional unit and said memory.

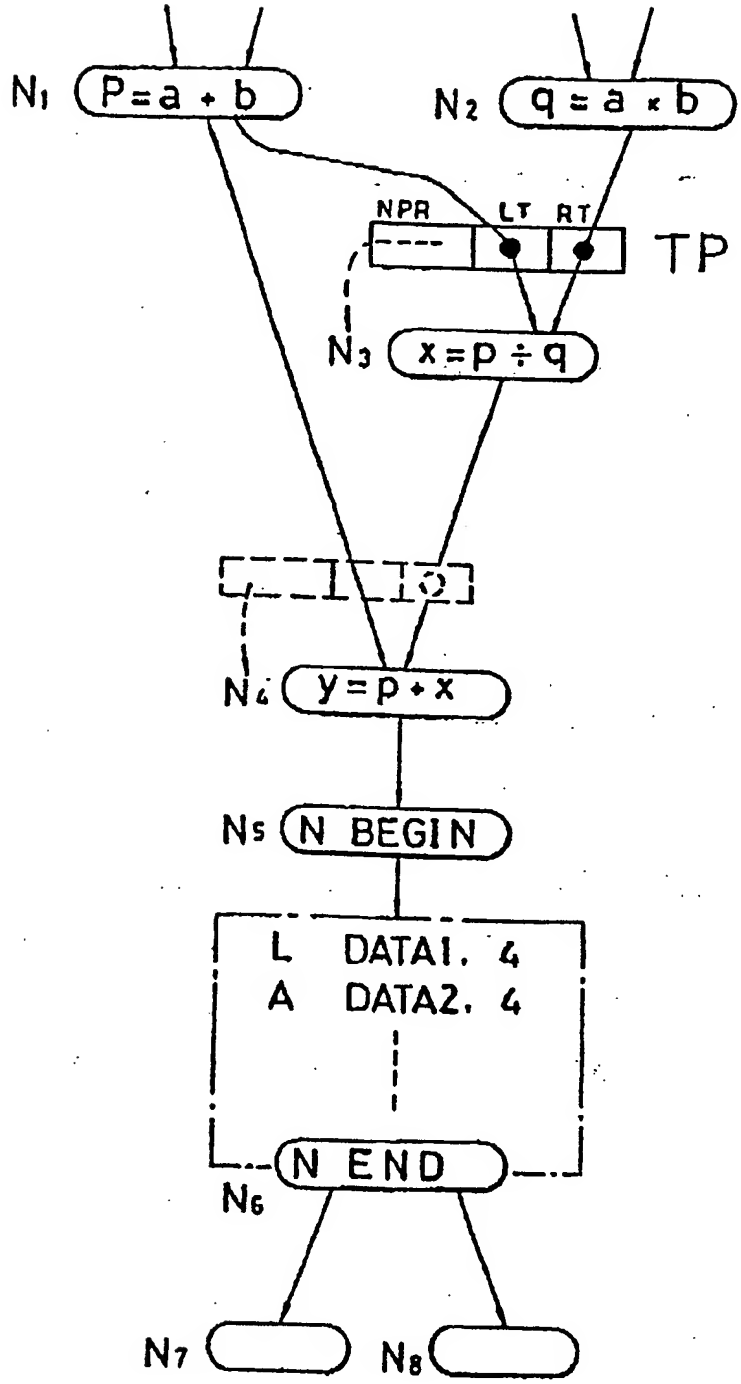
3. a parallel processing computer according to claim 1 or 2, wherein execution of instruction is controlled by token which represents simultaneously data to be used for executing said instruction.

FIG. 1



0144779

FIG.2



(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 144 779**
A3

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 84113431.5

(22) Date of filing: 07.11.84

(51) Int. Cl.⁴: G 06 F 9/44

(30) Priority: 07.11.83 JP 208567/83

(43) Date of publication of application:
19.06.85 Bulletin 85/25

(88) Date of deferred publication of search report: 10.07.85

(84) Designated Contracting States:
AT BE CH DE FR GB IT LI LU NL SE

(71) Applicant: Sowa, Masahiro
232-3, Hakoda-Cho
Maebashi-shi Gunma-ken(JP)

(71) Applicant: OMRON TATEISI ELECTRONICS CO.
10, Tsuchido-cho Hanazono Ukyo-ku
Kyoto 616(JP)

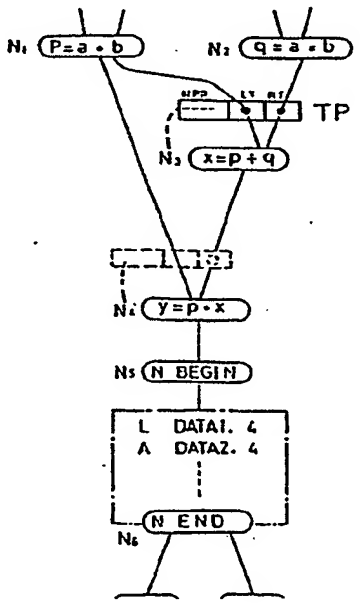
(72) Inventor: Sowa, Masahiro
232-3, Hakoda-cho
Maebashi-shi Gunma-ken(JP)

(74) Representative: WILHELMS & KILIAN Patentanwälte
Eduard-Schmid-Strasse 2
D-8000 München 90(DE)

(54) **Parallel processing computer.**

(57) A parallel processing computer comprises at least a memory for storing program as well as data and instructions for executing the program, a plurality of functional units, a node driving register for indicating executable instructions which are allowed to be executed by the functional units, and a mode register giving information to the functional unit as to whether the processing to be executed is of serial nature or parallel nature.

FIG.2



0 144 779 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application number: 0144778

EP 84 11 3431

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int Cl 4)
A	CONFERENCE PROCEEDINGS OF THE 10th ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, royal institute of technology, STOCKHOLM, (SE), 1983, pages 84-89 Computer society press, NEW YORK, (US), J.E. REQUE:"The piecewise data flow architecture control flow and register management". * Complete document * ---	1-3	G 06 F 9/44
P,A	EP-A-0 118 781 (SOWA, MASAHIRO)	1-3	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

G 06 F 9/44

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18-02-1985	LEPEE

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO Form 1503. 03 82